# 74LVC3G17-Q100

## Triple non-inverting Schmitt trigger with 5 V tolerant input

Rev. 5 — 24 August 2023 Product data sheet

## 1. General description

The 74LVC3G17-Q100 is a triple buffer with Schmitt-trigger inputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ±24 mA output drive ($V_{CC}$ = 3.0 V)
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Complies with JEDEC standards
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

## 3. Applications

- Wave and pulse shapers for highly noisy environments

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC3G17DP-Q100 | -40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74LVC3G17DC-Q100 | -40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |

# 5. Marking

**Table 2. Marking codes**

| Type number | Marking code [1] |
|---|---|
| 74LVC3G17DP-Q100 | V17 |
| 74LVC3G17DC-Q100 | V17 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

# 6. Functional diagram

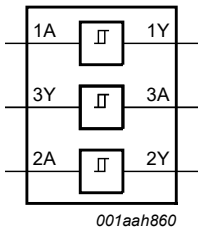



Fig. 1. Logic symbol

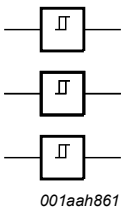



Fig. 2. IEC logic symbol

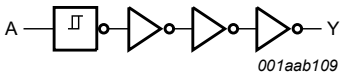



Fig. 3. Logic diagram (one gate)

# 7. Pinning information

## 7.1. Pinning

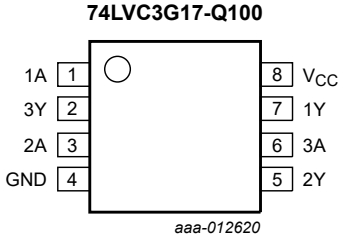



Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

### 7.2. Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1A, 2A, 3A | 1, 3, 6 | data input |
| GND | 4 | ground (0 V) |
| 1Y, 2Y, 3Y | 7, 5, 2 | data output |
| $V_{CC}$ | 8 | supply voltage |

## 8. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

| Input | Output |
|---|---|
| **nA** | **nY** |
| L | L |
| H | H |

## 9. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | -0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | -50 | - | mA |
| $V_I$ | input voltage | [1] | -0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ±50 | mA |
| $V_O$ | output voltage | Active mode [1] | -0.5 | $V_{CC}$ + 0.5 | V |
| | | Power-down mode; $V_{CC}$ = 0 V [1] [2] | -0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | - | ±50 | mA |
| $I_{CC}$ | supply current | | - | 100 | mA |
| $I_{GND}$ | ground current | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C [3] | - | 250 | mW |

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] When $V_{CC}$ = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.
[3] For SOT505-2 (TSSOP8) package: $P_{tot}$ derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: $P_{tot}$ derates linearly with 4.9 mW/K above 99 °C.

# 10. Recommended operating conditions

**Table 6. Operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | 5.5 | V |
| $V_I$ | input voltage | | 0 | 5.5 | V |
| $V_O$ | output voltage | | 0 | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | -40 | +125 | °C |

# 11. Static characteristics

**Table 7. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{T+}$ or $V_{T-}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.65 V to 5.5 V | - | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | - | - | 0.45 | - | 0.70 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | - | - | 0.3 | - | 0.45 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | - | 0.4 | - | 0.60 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.80 | V |
| | | $I_O$ = 32 mA; $V_{CC}$ = 4.5 V | - | - | 0.55 | - | 0.80 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{T+}$ or $V_{T-}$ | | | | | | |
| | | $I_O$ = -100 µA; $V_{CC}$ = 1.65 V to 5.5 V | $V_{CC}$ - 0.1 | - | - | $V_{CC}$ - 0.1 | - | V |
| | | $I_O$ = -4 mA; $V_{CC}$ = 1.65 V | 1.2 | - | - | 0.95 | - | V |
| | | $I_O$ = -8 mA; $V_{CC}$ = 2.3 V | 1.9 | - | - | 1.7 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.7 V | 2.2 | - | - | 1.9 | - | V |
| | | $I_O$ = -24 mA; $V_{CC}$ = 3.0 V | 2.3 | - | - | 2.0 | - | V |
| | | $I_O$ = -32 mA; $V_{CC}$ = 4.5 V | 3.8 | - | - | 3.4 | - | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V [2] | - | ±0.1 | ±1 | - | ±1 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 5.5 V; $V_{CC}$ = 0 V | - | ±0.1 | ±2 | - | ±2 | µA |
| $I_{CC}$ | supply current | $V_I$ = 5.5 V or GND; $I_O$ = 0 A; $V_{CC}$ = 1.65 V to 5.5 V [2] | - | 0.1 | 4 | - | 4 | µA |
| $\Delta I_{CC}$ | additional supply current | $V_I = V_{CC}$ - 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 2.3 V to 5.5 V [2] | - | 5 | 500 | - | 500 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.
[2] These typical values are measured at $V_{CC}$ = 3.3 V.

## 11.1. Transfer characteristics

**Table 8. Transfer characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $V_{T+}$ | positive-going threshold voltage | see Fig. 5 and Fig. 6 | | | | | | |
| | | $V_{CC}$ = 1.8 V | 0.70 | 1.10 | 1.50 | 0.70 | 1.70 | V |
| | | $V_{CC}$ = 2.3 V | 1.00 | 1.40 | 1.80 | 1.00 | 2.00 | V |
| | | $V_{CC}$ = 3.0 V | 1.30 | 1.76 | 2.20 | 1.30 | 2.40 | V |
| | | $V_{CC}$ = 4.5 V | 1.90 | 2.47 | 3.10 | 1.90 | 3.30 | V |
| | | $V_{CC}$ = 5.5 V | 2.20 | 2.91 | 3.60 | 2.20 | 3.80 | V |
| $V_{T-}$ | negative-going threshold voltage | see Fig. 5 and Fig. 6 | | | | | | |
| | | $V_{CC}$ = 1.8 V | 0.25 | 0.61 | 0.90 | 0.25 | 1.10 | V |
| | | $V_{CC}$ = 2.3 V | 0.40 | 0.80 | 1.15 | 0.40 | 1.35 | V |
| | | $V_{CC}$ = 3.0 V | 0.60 | 1.04 | 1.50 | 0.60 | 1.70 | V |
| | | $V_{CC}$ = 4.5 V | 1.00 | 1.55 | 2.00 | 1.00 | 2.20 | V |
| | | $V_{CC}$ = 5.5 V | 1.20 | 1.86 | 2.30 | 1.20 | 2.50 | V |
| $V_H$ | hysteresis voltage | ($V_{T+}$ - $V_{T-}$); see Fig. 5, Fig. 6 and Fig. 7 | | | | | | |
| | | $V_{CC}$ = 1.8 V | 0.15 | 0.49 | 1.00 | 0.15 | 1.20 | V |
| | | $V_{CC}$ = 2.3 V | 0.25 | 0.60 | 1.10 | 0.25 | 1.30 | V |
| | | $V_{CC}$ = 3.0 V | 0.40 | 0.73 | 1.20 | 0.40 | 1.40 | V |
| | | $V_{CC}$ = 4.5 V | 0.60 | 0.92 | 1.50 | 0.60 | 1.70 | V |
| | | $V_{CC}$ = 5.5 V | 0.70 | 1.02 | 1.70 | 0.70 | 1.90 | V |

[1] All typical values are measured at $T_{amb}$ = 25 °C.

## 11.2. Waveforms transfer characteristics

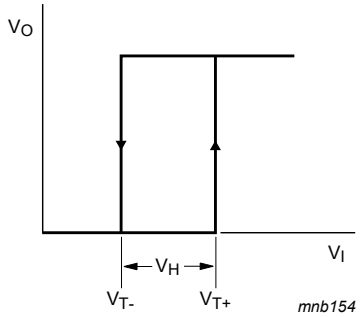
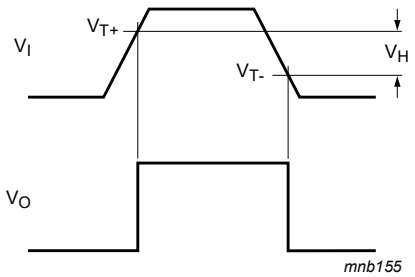
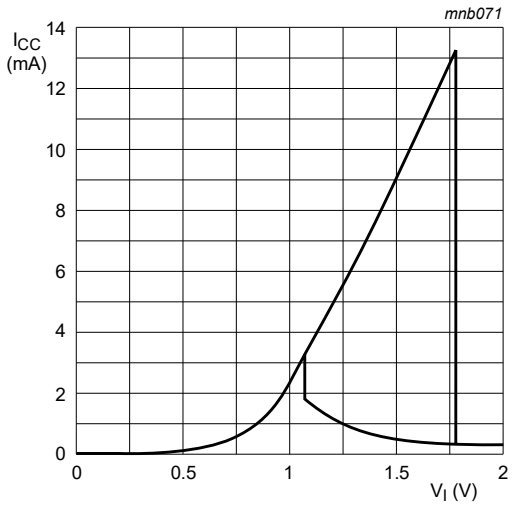



**Fig. 5. Transfer characteristic**



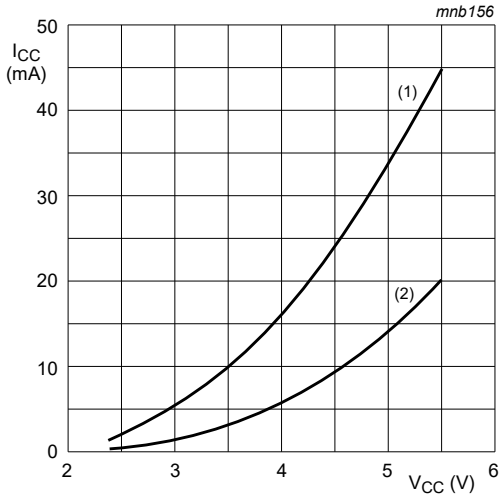

$V_{T+}$ and $V_{T-}$ limits at 70 % and 20 %.

**Fig. 6. Definition of $V_{T+}$, $V_{T-}$ and $V_H$**




$V_{CC}$ = 3.0 V.

**Fig. 7. Typical transfer characteristic**




(1) Positive-going edge.

(2) Negative-going edge.

Linear change of $V_I$ between 0.8 V to 2.0 V. All values given are typical unless otherwise specified.

**Fig. 8. Average $I_{CC}$ as a function of $V_{CC}$**

## 12. Dynamic characteristics

**Table 9. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nA to nY; see Fig. 9 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | 5.6 | 10.5 | 1.5 | 13.1 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.7 | 6.5 | 1.0 | 8.5 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 3.8 | 6.5 | 1.0 | 8.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.6 | 5.7 | 1.0 | 7.1 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | 2.7 | 4.3 | 1.0 | 5.4 | ns |
| $C_{PD}$ | power dissipation capacitance | per buffer; $V_{CC}$ = 3.3 V; $V_I$ = GND to $V_{CC}$ [3] | - | 16.3 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

$f_i$ = input frequency in MHz;

$f_o$ = output frequency in MHz;

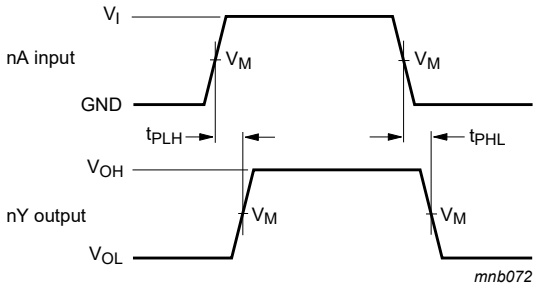
$C_L$ = output load capacitance in pF;

$V_{CC}$ = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

## 12.1. Waveforms and test circuit



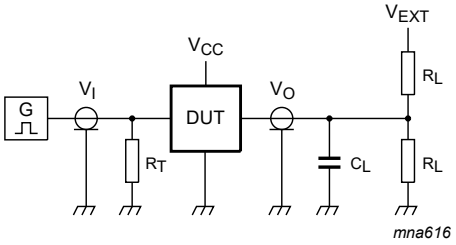

Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 9. The input (nA) to output (nY) propagation delays and the output transition times**

**Table 10. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ |
| 1.65 V to 1.95 V | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |
| 2.3 V to 2.7 V | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |
| 2.7 V | 1.5 V | 1.5 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V |
| 4.5 V to 5.5 V | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |




Test data is given in Table 11.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

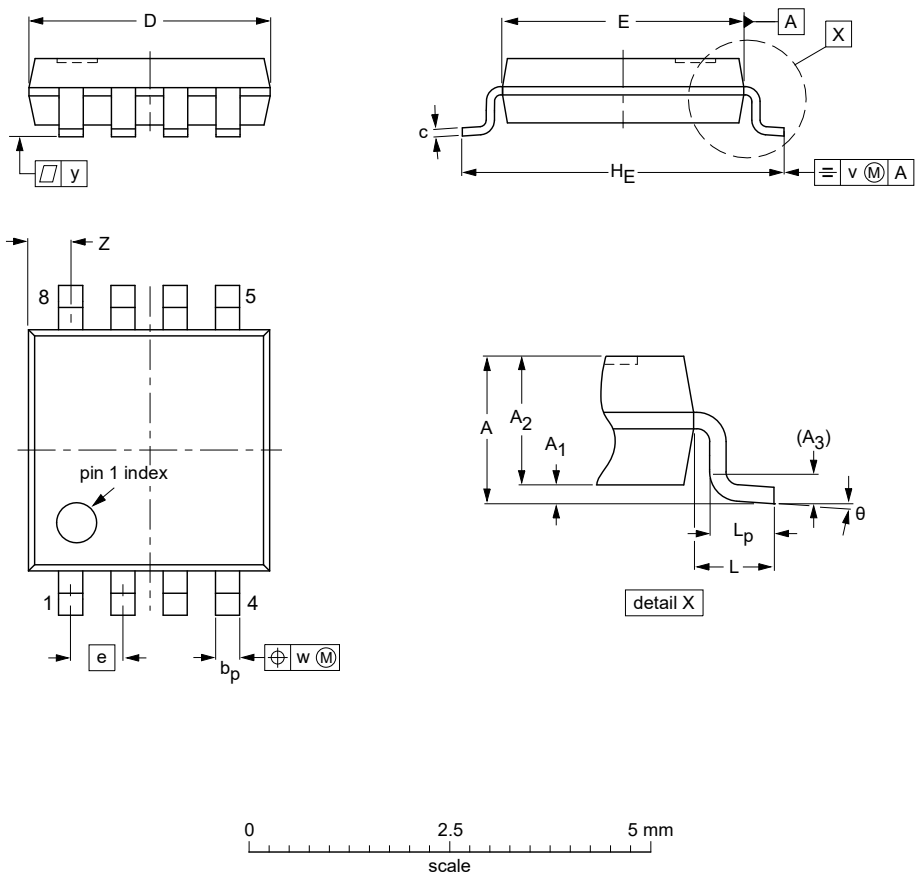
**Fig. 10. Test circuit for measuring switching times**

**Table 11. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 1 kΩ | open | GND | 2 × $V_{CC}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | GND | 2 × $V_{CC}$ |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 4.5 V to 5.5 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 2 × $V_{CC}$ |

## 13. Package outline

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.00 | 0.95<br>0.75 | 0.25 | 0.38<br>0.22 | 0.18<br>0.08 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 4.1<br>3.9 | 0.5 | 0.47<br>0.33 | 0.2 | 0.13 | 0.1 | 0.70<br>0.35 | 8°<br>0° |

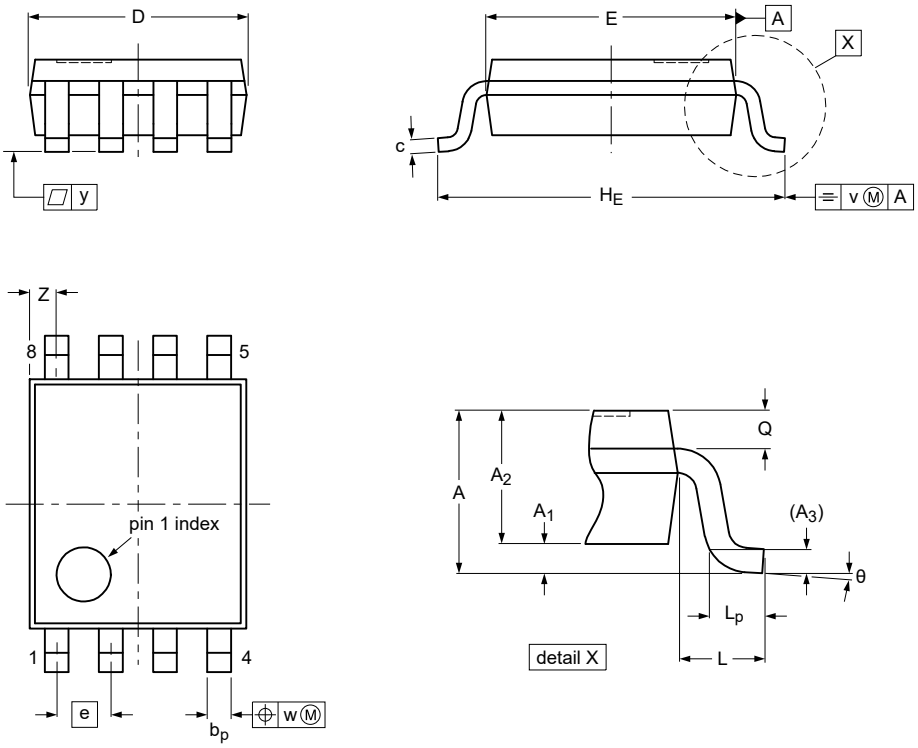
**Note**

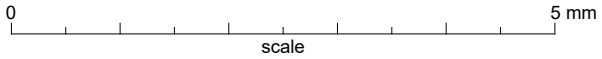
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | - - - | | | | 02-01-16 |

**Fig. 11. Package outline SOT505-2 (TSSOP8)**

**VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm** **SOT765-1**




Dimensions (mm are the original dimensions)

| Unit | | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1 | 0.15 | 0.85 | 0.12 | 0.27 | 0.23 | 2.1 | 2.4 | 0.5 | 3.2 | 0.4 | 0.40 | 0.21 | 0.2 | 0.08 | 0.1 | 0.4 | 8° |
| | nom | | | | | | | | | | | | | | | | | | |
| | min | | 0.00 | 0.60 | | 0.17 | 0.08 | 1.9 | 2.2 | | 3.0 | | 0.15 | 0.19 | | | | 0.1 | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

*sot765-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | ~~07-06-02~~ 16-05-31 |

**Fig. 12. Package outline SOT765-1 (VSSOP8)**

## 14. Abbreviations

**Table 12. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC3G17_Q100 v.5 | 20230824 | Product data sheet | - | 74LVC3G17_Q100 v.4 |
| Modifications: | • Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74LVC3G17_Q100 v.4 | 20210826 | Product data sheet | - | 74LVC3G17_Q100 v.3 |
| Modifications: | • Section 1 and Section 2 updated.<br>• Section 9: Derating values for $P_{tot}$ total power dissipation updated. | | | |
| 74LVC3G17_Q100 v.3 | 20181127 | Product data sheet | - | 74LVC3G17_Q100 v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74LVC3G17_Q100 v.2 | 20161214 | Product data sheet | - | 74LVC3G17_Q100 v.1 |
| Modifications: | • Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC3G17_Q100 v.1 | 20140522 | Product data sheet | - | - |

# 16. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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